A Sub-milliwatt 4–8 GHz SiGe Cryogenic Low Noise Amplifier

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***Abstract*—A 4-8 GHz Silicon-Germanium (SiGe) cryogenic low-noise amplifier (LNA) was designed and implemented using the Global Foundries BiCMOS8HP process. The amplifier provides 30-dB and 26-dB of gain while dissipating 760 μW and 580 μW DC power, respectively. The noise temperature is approximately 8 K across the frequency band. To the best of the authors' knowledge, this is the lowest reported power to date for a wide-band cryogenic integrated circuit LNA in this frequency range.**

***Index Terms*—Cryogenic low noise amplifier, low power, Silicon-Germanium (SiGe) heterojunction bipolar transistor (HBT).**

I. Introduction

Sub-milliwatt power consumption cryogenic low noise amplifiers (LNAs) are desired to enable THz kilopixel heterodyne cameras [1] using closed cycle refrigerators, which can support a maximum heat lift of 1.5 W at 4 K [2]. It was recently shown that Silicon-Germanium (SiGe) heterojunction bipolar transistors (HBTs) may be operated cryogenically at near optimum noise performance with collector–emitter voltages below 200 mV and a proof-of-concept 300 μW 2–4 GHz discrete transistor LNA achieving a noise temperature of 3–5 K and a gain greater than 25 dB was demonstrated [3]. Subsequently, a high gain discrete transistor amplifier was designed for direct integration with a 220 GHz superconductor-insulator-superconductor (SIS) mixer module. This amplifier operated over the 4–8 GHz frequency range and provided a power gain of 30 dB while consuming just 300 μW of DC power [4]. While the demonstration of discrete transistor amplifiers is an important step towards the development of scalable cryogenic receiver systems, integrated circuit amplifiers are desirable for the implementation of large systems. In this paper, a sub-milliwatt 4–8 GHz SiGe LNA MMIC is presented.

II. Design

A two-stage 4–8 GHz cryogenic low noise amplifier was designed using the low-V_{CE} SiGe HBT models reported in [3]. Emphasis during the design process was placed on a balance between noise, gain, return loss, and DC power. A schematic diagram of the amplifier appears in Fig. 1. To minimize losses, the input-matching network was realized external to the chip. The input stage features inductive degeneration to improve the power match and the input bond-wire has been absorbed into the matching network. The base of the input-stage transistor was biased through a shunt stub, with an AC ground provided by a 22 pF wire bondable capacitor. The emitter area of the first stage transistor was selected to be approximately 1.8 μm^2

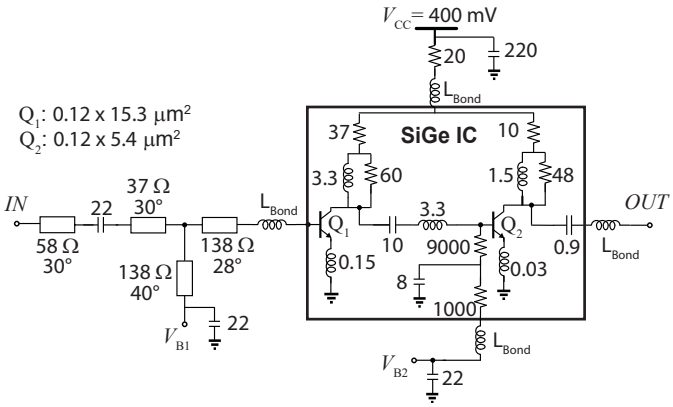


Fig. 1. A simplified schematic diagram of the low noise amplifier. The units are as follows: Resistors in Ω, Inductors in nH, Capacitors in pF. The electrical length of the transmission lines is specified at 6 GHz.

and the nominal bias current was set to 1.1 mA. These values were selected as a compromise between power consumption and noise match in the desired frequency range.

The interstage matching network was designed to flatten the gain while ensuring stability. The base of the second stage was biased through a low-pass resistive bias network.The output gain stage was implemented using an HBT with an emitter area of 0.65 μm^2 and biased at a nominal current of 0.8 mA. The output matching network was designed to provide a match to 50 Ω. An on-chip decoupling network (not shown in Fig. 1) was also included to permit the collectors of the first and second stage to share a single supply. The nominal value of V_{CC} was set to 400 mV, ensuring that both Q_1 and Q_2 were biased with sufficient headroom to achieve nominal noise performance.

The amplifier was simulated in the NI AWR design environment. Over the 4–8 GHz frequency range, the gain, return losses, and noise temperature were predicted to be better than 30 dB, 10 dB, and 6 K, respectively. These numbers are reported for the nominal power consumption of 760 μW. Detailed simulation results are reported in the following section along with the experimental data.

III. Experimental Results

The amplifier was implemented in the Global Foundries BiCMOS8HP technology process. A die photograph of the chip is shown in Fig. 2. The chip dimensions are 0.9 mm × 0.5 mm. Prior to packaging, on-wafer scattering

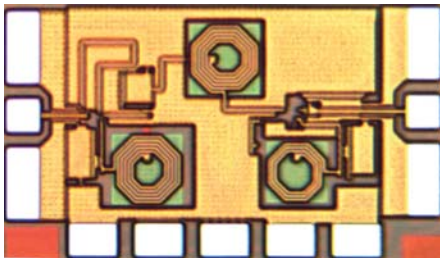


Fig. 2. Die photograph. The chip dimensions are 0.9 mm × 0.5 mm.

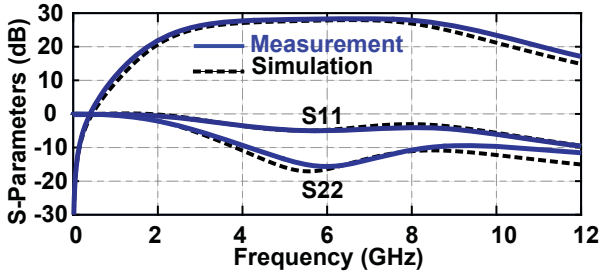
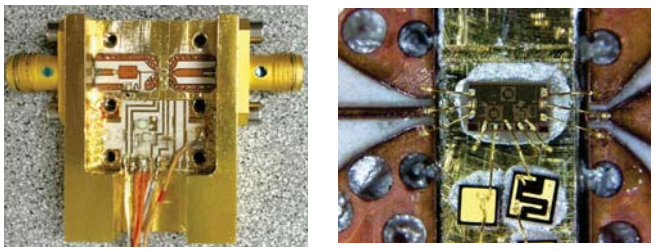


Fig. 3. On-Wafer scattering parameters of the amplifier at room temperature. Solid lines are measurements and dashed lines are simulation results.



(a) (b)

Fig. 4. The LNA assembly. (a) A photograph of the LNA package. (b) A close up picture of the LNA chip mounted inside the package.

parameter measurements of the integrated circuit were carried out. The room temperature measurements are compared to simulation results in Fig. 3. Excellent agreement between measurement and simulation was observed.

Following on-wafer measurements, the amplifier was packaged in a module for further testing. Photographs of the assembly appear in Fig. 4. The input and output matching networks were realized on separate RT/Duroid 6002 substrates, each with a thickness of 500 μm. These circuit boards were mounted in cutouts of 250 μm depth such that the surface of the RF boards were aligned that of the 250 μm thick silicon die, thereby permitting relatively flat wire-bond connections to be made between the printed circuit boards and the integrated circuit. The housing used in this work was initially designed to accommodate a slightly longer chip than that being tested here. Thus, relatively long bond-wires were required to connect between the chip and the input/output printed circuit boards (see Fig. 4(b)).

As a first step, noise figure and scattering parameter measurements of the amplifier were carried out at room temperature. The room temperature gain and noise performance is shown alongside simulation in Fig. 5. The measured gain was close to simulation and the noise figure was found to be approximately 0.5 dB higher than expected. This could be attributed to optimistic models for the off-chip input matching network. The input and output return losses of the packaged chip were also measured at room temperature and the results are consistent with simulation (see Fig. 6).

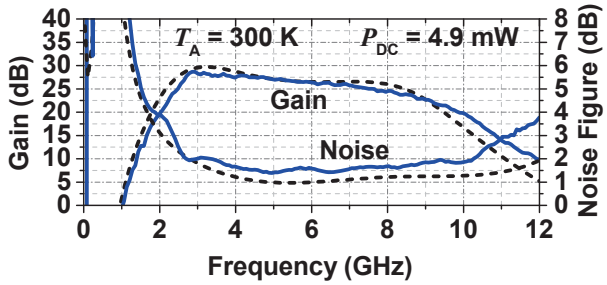


Fig. 5. Gain and noise figure measured at room temperature. The amplifier was biased at three times higher current density at room temperature in compare to 18 K in order to acheive the same transcunductance for the transistors. Solid lines are measurements and dashed lines are simulations.

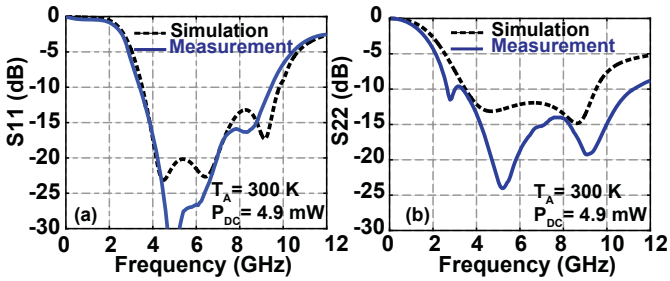


Fig. 6. Scatering parameters of the packaged amplifier at room temperature. Solid lines are measurements and dashed lines are simulation results. (a) Input reflection coefficient. (b) Output reflection coefficient.

After room temperature measurements, the cryogenic performance of the amplifier was characterized in a closed-cycle cryostat which has separate channels for scattering parameter and noise measurements. During the first measurement cycle, the amplifier was mounted for scattering parameter measurements and the return-losses of the amplifier were evaluated at a physical temperature of 18 K. The measured reflection coefficients, referenced to the plane of the vacuum feedthroughs at the edge of the cryostat wall appear alongside simulation results in Fig. 7. The input and output return losses were measured to be better than 11 and 12 dB, respectively. Moreover, the measured data were found to agree quite well with simulations. It should be noted that the ripple observed on the measurement may be attributed to the relatively long cables within the cryostat, which were not de-embedded from the results[1] and are required for thermal isolation.

Following scattering parameter measurements, the gain and

[1]The input and output cables contribute approximately 1 dB of loss, meaning that the error in the measurement of each reflection coefficient is believed to be well below 2 dB.

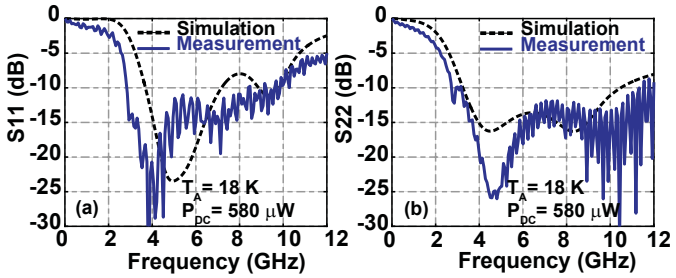


Fig. 7. Scatering parameters of the packaged amplifier at 18 K physical temperature. Solid lines are measurements and dashed lines are simulation results. (a) Input reflection coefficient. (b) Output reflection coefficient.

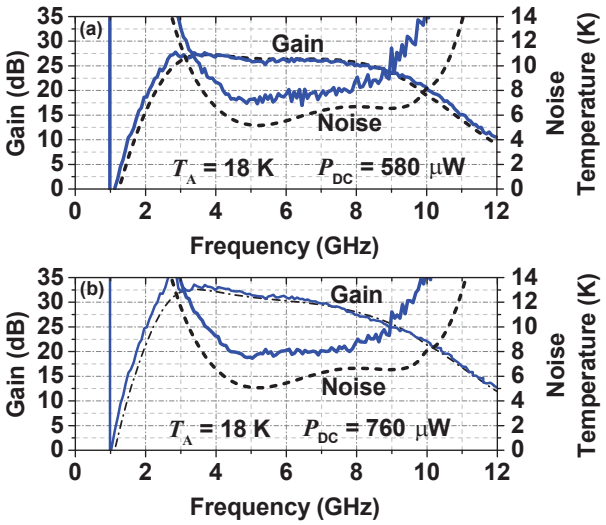


Fig. 8. Gain and noise temperature measured at 18 K physical temperature. Solid lines are measurements and dashed lines are simulation results. (a) The LNA was biased at 580 μW DC power. (b) The LNA was biased at 760 μW nominal power consumption.

noise of the amplifier was measured using the cold attenuator method [5]. Two sets of data were acquired; one with the LNA biased at its nominal bias point of $I_{C1} = 1.1\,\text{mA}$, $I_{C2} = 0.8\,\text{mA}$ and $V_{CC} = 0.4\,\text{V}$ and a second dataset with the second stage of the LNA biased at a reduced current of $I_{C2} = 0.35\,\text{mA}$. The corresponding power consumption for these two bias points was 760 and 580 μW, respectively.

The measured gain and noise temperature appear alongside simulation results in Fig. 8. At the nominal bias point (see Fig. 8b), the noise temperature in the 4–8 GHz frequency range was found to vary from 7.5 to 9.2 K, with an average value of 8 K. Over this same frequency range, the gain was found vary from 27.5 to 33 dB, with an average value of 30 dB. At the reduced-power bias point (see Fig. 8a), the gain flatness and noise performance were found to improve slightly, with the noise and gain ranging from 6.8–8.7 K and 25–27.3 dB, respectively. The average value of the gain and noise at this bias point were found to be 7.6 K and 26.1 dB, respectively. Referring again to Fig. 8, but now comparing measurement to simulation, it is apparent that the gain performance agrees quite well with simulation, but the measured noise temperature

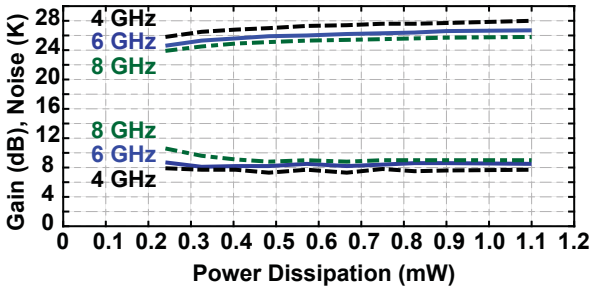


Fig. 9. Noise temperature and gain as a function of power dissipation at 4, 6, and 8 GHz frequency points. Collector voltage was swept from 700 mV to 200 mV for fixed base voltages.

TABLE I
STATE-OF-THE-ART CRYOGENIC MMIC LOW NOISE AMPLIFIERS

	Technology	Frequency GHz	Gain dB	Noise K	P_{DC} mW
[6]	InP HEMT	0.5-13	38-44	3-7	15
[7]	InPHEMT	4-12	27	13	5.7
[8]	mHEMT	4-12	31	5.3	8
[9]	mHEMT	4-12	26	8	12
This work	SiGe HBT	4-8	26	8	0.58

is about 1–2 K higher than expected. This could be due to an inaccurate model for the off-chip input matching network. Further work is required to understand this discrepancy.

The dependence of noise and gain on power consumption was also evaluated at a physical temperature of 18 K. These measurements were carried out with fixed base bias voltages corresponding to $I_{C1} = 1.1\,\text{mA}$ and $I_{C2} = 0.35\,\text{mA}$ when the supply voltage (V_{CC}) was set to 0.4 V. The power consumption was varied by sweeping the supply voltage from 700 mV to 200 mV. Over this range of supply voltages, the total current changed from 1.5 mA to 1.2 mA. The results of the measurement appear in Fig. 9. Remarkably, the noise below 6 GHz is nearly constant down to power levels as low as 230 μW. At the upper end of the band however, the noise increases marginally when the power is reduced below 400 μW. The gain was found to be weakly dependent upon power consumption, with a modest rolloff of about 2 dB observed over the $\approx 5:1$ range of power consumption. These results are quite encouraging, as they imply that the amplifier can provide excellent performance while operating with a DC power consumption well below 0.5 mW.

The amplifier performance is compared to other state-of-the-art cryogenic integrated circuit LNAs in Table I. The noise is similar to the other devices, but the power consumption is an order of magnitude lower than the other amplifiers.

IV. Conclusions

A 4–8 GHz cryogenic SiGe LNA that can be operated well below 600 μW has been demonstrated. To the best of the authors' knowledge, the power consumption achieved by this amplifier is the lowest to date for a high-gain wideband

cryogenic integrated circuit LNA. Future work should focus on the realization of amplifiers with similar power consumption and reduced noise as well as the demonstration of scalable systems built around these low power devices.

V. Acknowledgement

This work was partially supported by the NSF CAREER program through award number CCCS-1351744.

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