Manufacturable Cryogenic SiGe LNA for Radio Astronomy and Space Communications

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Abstract—This report presents results of recent work on the design of a wideband cryogenic low noise amplifier (LNA). The amplifier operates from 200 MHz to 6 GHz with noise temperatures of 2.8 K and 4.5 K at 1.6 GHz and 5.2 GHz respectively. The amplifier is designed for use as an easily manufacturable cryogenic amplifier for the Square Kilometer Array Wideband Single-Pixel Feed and holds promise as a general purpose cryogenic amplifier for radio astronomy, space communications, and low temperature physics research.

Index Terms—Cryogenic Low Noise Amplifier

I. Introduction

Designing cryogenic amplifiers has been an active area of research at Caltech for many years. Recent work has focused on the design of a cryogenic low noise amplifier from 1.6 to 5.2 GHz for the Square Kilometer Array (SKA) Wideband Single-Pixel Feed (WBSPF) technology development program. One of the major goals of this research was to design an easily manufacturable, inexpensive, very low noise cryogenic amplifier as the SKA requires hundreds to thousands of amplifiers. These goals have been achieved and this report summarizes the design process and results for a cryogenic SiGe amplifier with 2.8 and 4.5 K noise at 1.6 and 5.2 GHz respectively.

II. Understanding SiGe transistors

Silicon Germanium (SiGe) cryogenic amplifiers have several advantages compared to traditional cryogenic High Electron Mobility Transistor (HEMT) amplifiers. SiGe is a readily manufacturable process with very good repeatability. Due to their bipolar structure, SiGe devices have better input match at low frequencies and extremely low minimum noise temperatures (~ 1K), making the technology an excellent choice for cryogenic amplifiers below 8 GHz. For this design the applicable transistors were very high performance (380 GHz Fmax), silicon gemanium (SiGe) bipolar transistors commercially available from ST Microelectronics as the BICMOS055 process [1,2].

This allows the design to be readily fabricated with commercially available components as the transistors come from a standard ST process. Fig. 1 shows a Medium Frequency 5GHz (MF5) amplifier using an ST type 055HS transistor as the first stage. The three stages are cascaded from left to right.

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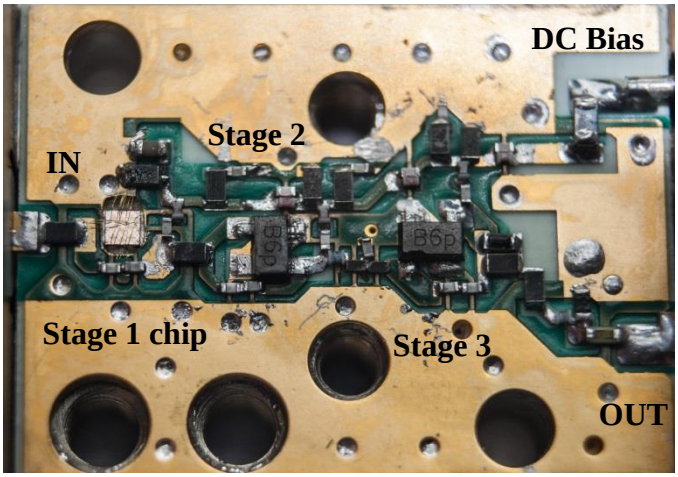

Fig. 1. Layout of an MF5 amplifier used for cyrogenic testing. The circuit board is 15.8 x 20.5 mm. An ST Microelectronis chip transistor is used for the first stage while NXP BFU725 packaged tranistors are used for stages 2 and 3.

One advantage of SiGe transistors during the design process is that the low frequency limit of all four of their noise parameters can be accurately predicted at any temperature using simple DC measurements at that temperature as shown by Weinreb [3]. This provides significant design insight compared with HEMTs as measuring the cryogenic noise parameters of a transistor directly is inherently a difficult and often tedious measurement. For a SiGe transistor the minimum noise temperature T_{min} can be predicted by measuring the current gain, beta, of the transistor, the transconductance, gm, and the base resistance as a function of collector current. T_{min} is the minimum noise temperature that the device will add when the generator impedance is optimally matched for lowest noise. Usually the base resistance is small enough that its noise contribution to T_{min} can be neglected to first order at cryogenic temperatures below 20K. The resulting T_{min} equation given below where q is the charge of an electron, k_B is Boltzmann's constant, gm_o is the ideal gm, T_o is 290K, and gm, Ic, and beta are the measured values of those parameters at any physical temperature [3].

$$T_{min} \approx \frac{q*I_C}{k_B*gm*\sqrt{\beta}} = T_o * \frac{gm_o/gm}{\sqrt{\beta}} \quad (1)$$

$$gm_o = \frac{Ic}{.025V} \quad (2)$$

Since T_{min} changes with bias, one must plot T_{min} as a function of bias current and design the device for operation at the optimal bias point for minimum noise. The underlying mechanism for noise in a SiGe transistor is shot noise at the base and collector junctions due to the random movement of electrons across the junction and thermal noise due to the base resistance [3]. Significant noise contributions from other first stage components can also add additional noise to that from the transistor itself.

Fig. 2 shows T_{min}, T_{50}, and $R_{opt}/50$ vs collector bias current as these parameters are used to optimize the bias current when starting a design. T_{50}, is the minimum noise temperature produced when the input is a 50 ohm source. $R_{opt}/50$ is the normalized optimal impedance with respect to 50 ohms. The R_{opt}impedance is real for frequencies below a few GHz. For best performance one should design the amplifier such that $R_{opt}/50 \approx 1$ so that a wideband optimal noise match can be achieved with a 50 ohm input without the need for an impedance transformation network.

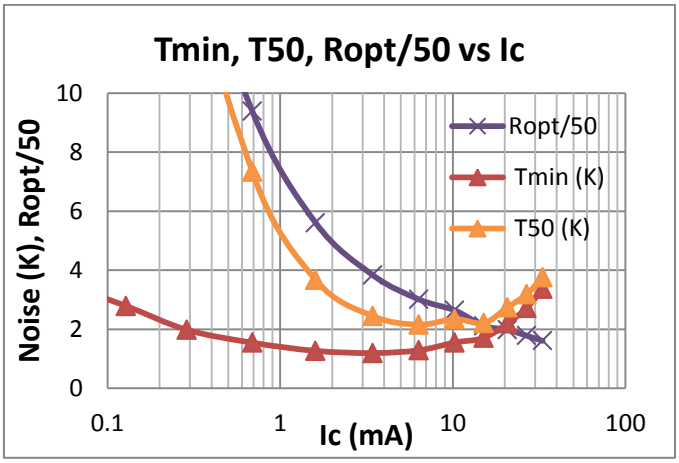

Fig. 2. Theoretical prediction for $R_{opt}/50$, T_{min}, and T_{50} for a ST 055HS transistor with 4.45 um emitter area at 21K using the measured values of beta, gm, and Rb.

Note that in this low frequency limit and with negligible thermal noise from Rb, the noise reduction at cryogenic temperatures is due only to increases in gm and beta. Typical values for the ST 055HS transistor are 12,000 for beta and 1 A/V for gm at 20K. As is apparent from Fig. 2, all of these parameters change with bias current which gives the designer some control over the noise parameters. If the device R_{opt} is much higher than 50 ohms, then the designer can put multiple devices in parallel, effectively reducing the optimum generator impedance by 1/n where n is the number of devices in parallel. Amplifier modeling was performed using a combined cryogenic small signal model and noise model of each transistor, a model of each passive component, and a Microwave Office microstrip element model for every length of connecting trace. The measurement procedure used to extract the small signal values cryogenically is outlined in detail by Bardin in [4].

MF5 amplifier modules were assembled and tested with several first stage transistors. Some of the best results were obtained with the ST 055HS transistors with 4.45um effective area which was the largest transistor size in our test reticule. Fig. 2 implies that R_{opt} is is much greater than 50 ohms when the transistor is biased at its optimal bias current of 3-4 mA. To improve the noise match 3 transistors on the same reticule with effective emitter areas of 4.45, 3.56, and 2.67 um^2 were placed in parallel giving a total area of 10.7 um^2 to reduce the effective R_{opt} impedance. The transistors were connected using a wire bond stitching technique shown in Fig. 3. Due to the long bond wire lengths associated with this design, the amplifier oscillated when measured at room temperature but surprisingly was stable when cold.

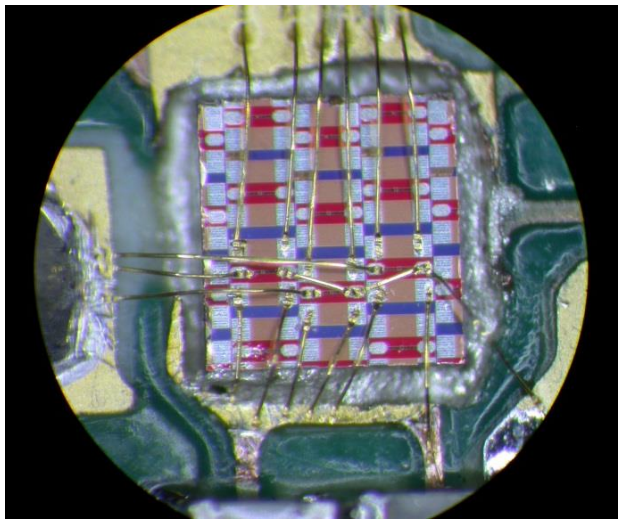

Fig. 3. View of the wirebonding of three parallel ST BiCMOS055HS transistors inside the MF5 amplifier shown in Fig. 1.

The amplifier was designed as the combination of three cascaded gain stages in series with high pass filter networks to achieve reasonable gain flatness. Output attenuation was added to achieve better S22 return loss. Each stage is composed of a common emitter amplifier with a feedback resistor from collector to base to provide bias and improve the input return loss. The circuit design is based on previous work outlined in [5] and a schematic is shown in Fig. 6.

III. Measured Results

Measured and modeled noise for two MF5 amplifiers is shown in Fig. 4, and cryogenic S parameters for a MF5 amplifier are shown in Fig. 5. Depending on the effective area of the transistor used in the amplifier, the noise match and thus the noise performance will be better at the low or high end of the band. Fig. 4 highlights this, showing measured results which are noise matched at different ends of the band. There are some discrepancies between the measured noise data and the noise model and it is believed this is due to three main factors. First, the noise measurement setup used is only accurate to ± 1 K. Second, the passive components in the circuit may have more complex models than have been used. Third, the model may not account for all of the noise mechanisms in the transistors.

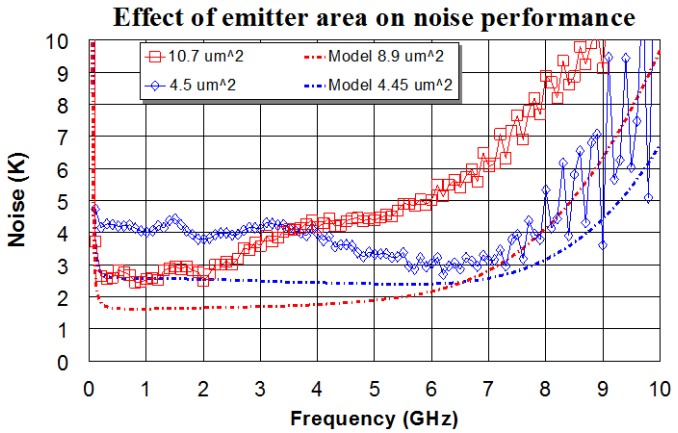

Fig. 4. Modeled and measured noise of two MF5 amplifiers with different first stage emitter areas.

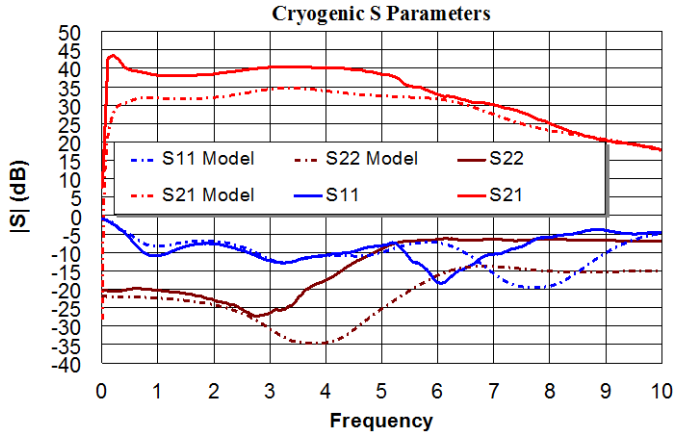

Fig. 5. Measured and modeled cryogenic S parameters S11, S21, and S22 for a MF5 amplifier using a ST055HS tranistor with 4.5 um emitter area.

Fig. 5 shows measured and modeled S11, S21, and S22 for a cryogenic amplifier using a single 4.45um ST055HS transistor. The model used to design the amplifier accurately predicts these measured responses up to 2.5GHz for S22, up to 5.2 GHz for S11 and up to 10 GHz for S21. The model used did not account for the transistor's parasitic inductances and thus measured results diverge as the frequency increases. The gain differences between the measured data and the model can be reduced by reducing the modeled emitter inductance of the first stage transistor. This alone raised the modeled gain by 5dB across the band. Although most of the components can be accurately modeled before designing the amplifier, the first stage emitter inductance is very difficult to model as a small change in the bond wire length can create a significant change in emitter inductance. As the chip is wire bonded by hand, some variability is inevitable. The emitter inductance plays a key role in achieving noise matching and gain, especially as frequency increases above a few GHz.

IV. Conclusions

This report has presented preliminary measurement results for a manufacturable low noise cryogenic amplifier with applications in radio astronomy, communications, and low temperature physics research. Future work will investigate the design of higher frequency SiGe cryogenic amplifiers, improved noise modeling of the first stage transistor, and optimized narrow band amplifiers for specific applications.

Acknowledgment

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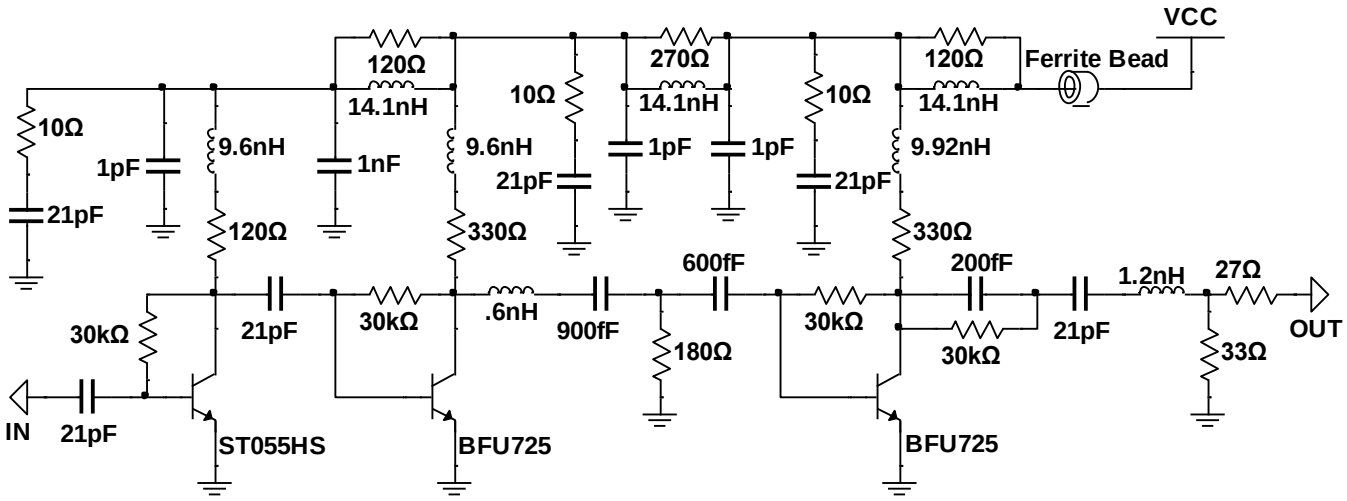

Fig. 6. Schematic of the MF5 amplifier excluding microstrip transmission lines. All tests reported here are for a single supply voltage of 2.5 volts and current of 14.5 mA for the single transistor version and 20.3 mA for the 3 transistor parallel version at 20K.

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