



# Evaluation of biasing and protection circuitry components for cryogenic MMIC low-noise amplifiers



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## ABSTRACT

Millimeter-wave integrated circuits with gate lengths as short as 35 nm are demonstrating extremely low-noise performance, especially when cooled to cryogenic temperatures. These operate at low voltages and are susceptible to damage from electrostatic discharge and improper biasing, as well as being sensitive to low-level interference. Designing a protection circuit for low voltages and temperatures is challenging because there is very little data available on components that may be suitable. Extensive testing at low temperatures yielded a set of components and a circuit topology that demonstrates the required level of protection for critical MMICs and similar devices. We present a circuit that provides robust protection for low voltage devices from room temperature down to 4 K.

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## 1. Introduction

Microwave/millimeter-wave monolithic integrated circuits (MMICs) with gate lengths as short as 35 nm are proving to be very low noise amplifiers in the region of 100–300 GHz at room temperature, with significant reduction in noise being observed on cooling to a few kelvin [1]. The very small, sensitive transistors operate at supply voltages less than a volt and currents of a few milliamperes and require protection from excessive voltages and currents, even at operating temperatures as low as 4 K. In addition to damage protection, mitigation of interference is important. Interference can come from many sources, such as wireless networks, other electronics in the system, and switch-mode power supplies. Interference out of the nominal amplifier band can cause overloading, amplitude instability, or intermodulation products that may cause more or less significant data degradation depending on the application. This problem becomes acute in the context of these millimeterwave amplifiers because the low-voltage operation limits the saturation power, while the wide bandwidth results in relatively high total power for a given power density required to exceed the noise floor of following stages.

While it is common practice to place the protection and filtering circuitry remote from the MMIC, at room temperature, for several reasons it is more reliable and robust if the protection can be integrated in the same package as the MMIC chips. Having the

protection in the block protects the amplifier from the time of assembly. This is particularly valuable in a university environment where they are commonly used by students without a background in handling sensitive components. It also protects against possible problems with wiring inside a cryostat. Another benefit that we have experienced is reduction of radiative coupling from other wires inside a cryostat. Filtering within the amplifier block rejects this type of interference. Some components in the bias network, particularly capacitors and resistors, act as both protection and filtering devices.

CARMA (Combined Array for Research in Millimeter-wave Astronomy [2,3]) is developing a new generation of MMIC amplifiers to cover the range 80–116 GHz for radio astronomy. Twenty-three antennas with dual-polarization receivers will require about 60 amplifiers or 180 MMIC chips (three per amplifier). To conserve the limited supply of chips over many years of operation we need to incorporate reliable protection into the amplifiers. The goal was to base the protection and filtering on low-cost commercial components.

A review of the literature did not reveal any designs of circuit protection and bias networks that meet the stringent requirements of low voltages at cryogenic temperatures, and no data to demonstrate the suitability of all necessary components that can be used in a design. Even without considering cold operation, ESD protection devices are generally designed for voltages higher than the safe limit for this new generation of MMICs.

To develop a new protection scheme for our devices we had to test a broad range of components and design a circuit based on the

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measured characteristics. In the following section we present the results of device testing, followed by a description of a circuit based on the most appropriate components. Finally, we show some measurements that demonstrate that the circuit is indeed capable of preventing fast, high-voltage transients from reaching the susceptible components.

## 2. Brief survey of published measurements

There is limited information available on the properties of commercial electronic components at cryogenic temperatures. We summarize some of the published data, but since this type of information is often a subsidiary part of a publication we cannot guarantee that it is a complete survey. The range of components mentioned is greater than required in this application, but given the paucity of information it was considered useful to collect it in a single place. One of the primary uses for low-temperature electronics is in space missions (see the review by Patterson et al. [4], for example), so much of the literature is from that field. The following selection is presented in roughly historical sequence.

For a spaceborne infrared camera, Stefanovich et al. [5] found a Type 2 ceramic capacitor that had a capacitance at 4 K of 15 pF, a tenth of the room temperature value; they did not specify the part number or footprint. Additionally, they investigated several active devices (J-FETs and MOSFETs).

Surface-mount ceramic and solid tantalum capacitors in the range 0.1–10  $\mu$ F were evaluated down to 77 K by Hammoud et al. [6]. Three types of tantalum capacitor lost about 75% of their capacity, while the two ceramic-CRX capacitors showed an increase in capacitance by factors of 2.3 and 4.5. Their data also include frequency and temperature dependence of the capacitance and dissipation factor. The same group later tested a different set of capacitors [7] (polypropylene, polycarbonate, solid tantalum, mica, and electric double layer) having a similar range of capacitances. All these had stable capacitances to 77 K within a few percent. The solid tantalum showed an increase in dissipation factor at low temperatures.

Gerber et al. [8] studied the effect of temperature on four magnetic-core inductors of about 10  $\mu$ H down to 93 K. Two of the core materials caused a reduction of the inductance by 40–80%, while two were substantially unchanged.

Some interesting developments of cryogenic-specific capacitors are reported by Alberta and Hackenberger [9]. They discuss optimization for three applications; low temperature coefficient, high volumetric efficiency, and energy storage. Stable capacitors with values up to 62 nF were developed, but there is no indication if these components were put into commercial production.

In a study for Martian surface applications, Tugnawat and Kuhn [10] examined a series of on-chip passive components down to 153 K, observing variations in component values of order 10%. The integrated nature of the devices made them unsuitable for our needs, however.

Several types of resistor were characterized by Bourne et al. [11] for DC motor drives. Thin-film, thick-film, wire-wound, and foil resistors were all found to maintain their resistance values to 90 K, while carbon composition and ceramic composition devices changed by  $\sim$ 25%. In the same study, commercial polypropylene, polyethylene, NPO ceramic, mica, and polyester capacitors had stable capacitances to within  $\pm$ 5%, with the NPO having the lowest variation at  $\leq$ 1%. Typical values selected were of order 1  $\mu$ F, and the packages were relatively bulky through-hole implementations. Testing also included various kinds of diode (Schottky, switching, PIN, point contact and Zener, in Si, GaAs, or Ge). In general, all showed some increase in the forward turn-on voltages and reduction in the conducting region resistance.

A useful set of data on the mechanical properties of materials has been published by Fink et al. [12], covering solders and PCB materials. The circuits we are developing are small and in a relatively benign environment (infrequent thermal cycles with slow rates of change, and low vibration) and not particularly vulnerable to cryogenic stress, but for more extreme conditions, such as spacecraft environments, this information may be very valuable.

Finally, we note the results presented by Buchanan et al. [13] for a variety of commercial components at 4.2 K. In addition to some active devices (amplifiers, FETs, analog switches, and logic elements) they identify temperature stable resistors by Vishay. The DC bypass capacitor they use is a KEMET [14] X7R that drops from 100 nF to 5 nF at 4.2 K. A Dialight [15] RL50 LED (light-emitting diode) was shown to work at low temperature, with a conduction voltage that changed from 1.6 V to 1.9 V at 4.2 K.

## 3. Component selection and characterization

Since the publications listed above did not yield a complete set of components that meet our particular needs, we compiled a set of devices to test, based on: commercial availability, footprint size, package type, and cost. Testing had to demonstrate useful behavior down to  $\sim$ 4 K.

A simple set of procedures was used to characterize the temperature dependence of the components. They were mounted on a circuit board that could hold up to six devices. Signal traces and a common ground trace went to a 9-pin D-sub connector. The board was mounted on a copper block that was either immersed in liquid nitrogen (LN) or attached to the cold plate in a 4-kelvin closed-cycle refrigerator.

Both sides of the board had copper planes on them to minimize any temperature gradients, with vias connecting the top and bottom planes electrically and thermally. A temperature sensor was affixed to the copper plate, and it is conceivable that there could be a temperature differential between the sensor and the components. However, in the sense that this type of construction is representative of how the components are to be used, it was felt that this was a valid test configuration, and in any case temperature differences at the level of a few kelvin are expected to be inconsequential.

As discussed below, some modifications were made to the procedure for the capacitor tests.

### 3.1. Resistors

Resistors are required to limit current into sensitive components, such as transistor gates, or to divide down voltages so that external noise or interference is reduced. Combined with capacitors, they form low-pass filters to reject high-frequency noise. Typically, the required tolerances on the resistance are not extremely tight, and an accuracy of  $\sim$ 2%, comprising 0.5% manufacturing tolerance and 1.5% temperature variation, is usually acceptable. Manufacturing tolerances of modern thin-film resistances are very good, and the cost of 0.5% resistors is very low.

Resistance in conductors is due to collisions of electrons with impurities, lattice defects, or phonons (see, for example, [16]), or by boundaries [17]. The most temperature dependent process is phonon scattering which causes the resistivity to vary at a rate between  $T$  and  $T^5$  [16]. Such sensitivity is unacceptable for resistors, so they are composed of materials with impurities and/or lattice defects such that the thermal phonon scattering is a minor contribution. For sufficiently low impurity concentration the temperature dependence approaches zero. Boundary scattering is important only for thicknesses  $\leq$  300 nm for pure metals. Thin film resistors have thicknesses  $\leq$  100 nm, but use higher resistivity

materials where the bulk material mean free path is less than the film thickness. Commonly used materials include NiCr, TaN and SiCr, which have much higher bulk resistivity than pure metals. Campbell and Morley quantify thin film resistivity in terms of the ratio of thickness to mean free path [18]; the results are to extensive to repeat here, but the main conclusion is that there are no strongly temperature dependent terms.

In practical terms, the precise behavior depends also on dimensional changes in the material, the substrate roughness, and deposition and annealing details. Commercial production focuses on stability since the accuracy is ensured by laser trimming. It can reasonably be expected that a resistor with low variation in the normal commercial temperature range will still perform well at cryogenic temperatures. Possible exceptions are catastrophic failure due to cracking, or a superconducting transition (unlikely). Some manufacturers specify their components to work down to 77 K, but these typically come in a smaller range of resistances and packages, and are more expensive than standard components. The range produced by Vishay Precision Resistors [19] is a good example of precision resistors that work well cryogenically.

We tested several inexpensive commercial thin-film SMT resistors down to 4 K to see if they were suitable for moderate accuracy applications (Table 1). Although not listed in this table, other thin-film resistors from different manufacturers that we have measured at various times all have similar temperature characteristics.

Resistances were measured with a Fluke 87 III multimeter [21]. A separate cool down of the test block with short circuits in place of the resistors yielded a value for the wiring resistance. This was about 11.86 Ω at room temperature and decreased by only ~0.2 Ω when the short-circuit end was cooled to 4.2 K in the measurement configuration.

All the resistors measured (Table 2) exhibited changes of ≤1%, apart from the 9.09 kΩ resistors, which changed by ~4% at 4 K (although one sample, no. 17 in Table 1, was very stable). These are shown graphically in Fig. 1.

3.2. Capacitors

Capacitors are primarily used to filter out noise from external sources, and to ensure low impedance termination of the bias lines at frequencies where amplifiers may be prone to oscillation. A wide range of capacitance values may be required; small capacitors with high self-resonant frequencies placed near the active devices, and larger capacitor with lower resonant frequencies farther away. Values below a picofarad or so are generally incorporated on the MMIC chip itself. In the ≤100 pF range, wire bonded capacitors

Table 2

Room temperature and cryogenic measurements of the resistors listed in Table 1. Changes in resistance are shown relative to the room temperature value.

No.	R, RT	R, 77 K	Δ (%)	R, 4 K	Δ (%)
1	50.81 Ω			50.27 Ω	-1.06
2	50.99 Ω	50.75 Ω	-0.47	50.51 Ω	-0.47
3	820.4 Ω	819.1 Ω	-0.16	818.8 Ω	-0.04
4	1.000 kΩ			0.998 kΩ	-0.20
5	1.000 kΩ	0.997 kΩ	-0.25	0.997 kΩ	-0.09
6	1.001 kΩ	0.998 kΩ	-0.30		
7	1.002 kΩ	0.998 kΩ	-0.40	0.998 kΩ	-0.40
8	1.011 kΩ	1.009 kΩ		1.008 kΩ	
9	4.020 kΩ	4.010 kΩ	-0.25		
10	4.028 kΩ	4.018 kΩ		4.015 kΩ	
11	4.030 kΩ	4.010 kΩ	-0.50		
12	4.030 kΩ	4.030 kΩ		4.032 kΩ	
13	8.20 kΩ	8.274 kΩ	0.86	8.526 kΩ	3.05
14	9.07 kΩ	9.15 kΩ	0.88	9.452 kΩ	4.21
15	9.07 kΩ	9.06 kΩ	-0.11		
16	9.087 kΩ	9.154 kΩ	0.72	9.418 kΩ	2.91
17	9.095 kΩ	9.084 kΩ		9.095 kΩ	
18	9.995 kΩ	10.108 kΩ	1.13	10.509 kΩ	3.97

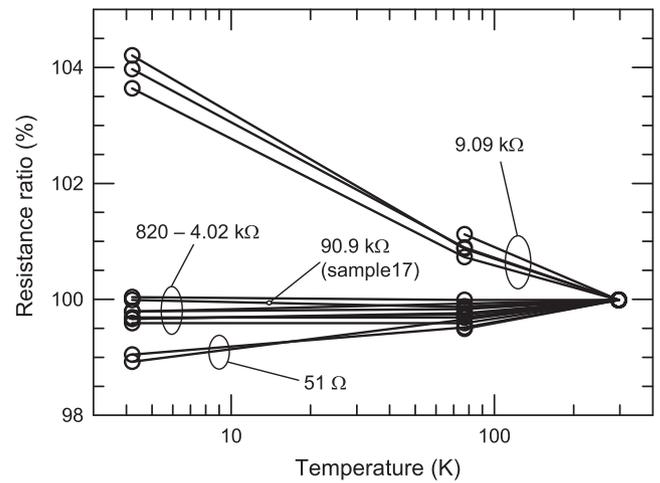


Fig. 1. Changes in resistance as a function of temperature for the components listed in Table 1. These generally cluster according to the resistance value.

can be placed on the amplifier block, very close to the chip, while larger value components (≤100 nF) can be mounted on conventional FR4 printed circuit board. HEMTs have gain down to DC, and by definition the bias lines are DC coupled, so it is important

Table 1 Resistors selected for cryogenic testing.

No.	Manuf.	P/N	Value	Power (W)	Tol. %	Temp. coeff. (ppm/°C)	Package
1	SUSUMU [20]	RG1005P-510-D-T10	51 Ω	0.063	0.5	±25	0402
2	SUSUMU	RR0510P-510-D	51 Ω	0.063	0.5	±25	0402
3	SUSUMU	RR0510P-821-D	822 Ω	0.063	0.5	±25	0402
4	SUSUMU	RG1005P-102-D-T10	1.00 kΩ	0.063	0.5	±25	0402
5	SUSUMU	RR0510P-102-D	1.00 Ω	0.063	0.5	±25	0402
6	SUSUMU	RR0816P-102-D	10 kΩ	0.063	0.5	±25	0603
7	SUSUMU	RR0510P-102-D	1.00 kΩ	0.063	0.5	±25	0402
8	SUSUMU	RR0816P-102-D	1.00 kΩ	0.063	0.5	±25	0603
9	SUSUMU	RR0510P-4021-D	4.02 kΩ	0.063	0.5	±25	0402
10	SUSUMU	RR0510P-4021-D	4.02 kΩ	0.063	0.5	±25	0402
11	SUSUMU	RR0816P-4021-D-59H	4.02 kΩ	0.063	0.5	±25	0603
12	SUSUMU	RR0816P-4021-D	4.02 kΩ	0.063	0.5	±25	0603
13	SUSUMU	RR0510P-822-D	8.22 kΩ	0.063	0.5	±25	0402
14	SUSUMU	RR0510P-9091-D	9.09 kΩ	0.063	0.5	±25	0402
15	SUSUMU	RR0816P-9091-D-93H	9.09 kΩ	0.063	0.5	±25	0603
16	SUSUMU	RR0510P-9091-D	9.09 kΩ	0.063	0.5	±25	0402
17	SUSUMU	RR0816P-9091-D	9.09 kΩ	0.063	0.5	±25	0603
18	SUSUMU	RR0510P-103-D	10.0 kΩ	0.063	0.5	±25	0402

to avoid feedback between drain and gate; we have encountered devices that required  $\sim 100$  nF bypass capacitance close to the amplifier to ensure stability.

A parallel plate capacitor of plate area  $A$  and separation  $d$  having a dielectric constant  $\epsilon$  has a capacitance of:

$$C = \epsilon \frac{A}{d}. \quad (1)$$

The dependence on temperature,  $T$ , is characterized by the temperature coefficient of capacitance [22],

$$\gamma_c = \frac{1}{C} \left( \frac{\partial C}{\partial T} \right)_p. \quad (2)$$

Although the partial derivative is taken at constant pressure, the change in pressure from ambient to vacuum can safely be ignored.

The Lorentz–Lorenz relationship [23] (also known as the Clausius–Mosotti relationship) relates the permittivity,  $\epsilon$ , to the macroscopic polarizability,  $\alpha_m$ , of a small macroscopic volume  $V$ :

$$\frac{\epsilon^2 - 1}{\epsilon^2 + 1} = \frac{4\pi}{3} \frac{\alpha_m}{V}, \quad (3)$$

and the capacitance temperature coefficient is then found to be [24,25]:

$$\gamma_c = \frac{(\epsilon - 1)(\epsilon + 2)}{\epsilon} \left( \frac{1}{3\alpha} \left( \frac{\partial \alpha_m}{\partial T} \right)_p - \alpha_1 \right) + \alpha_1. \quad (4)$$

$\alpha_1$  is the linear coefficient of thermal expansion of the dielectric. The second term quantifies the change in permittivity from the variation in number density of dipoles, while the third term represents the counteracting change due to the dimensions in (1). If  $\alpha_m$  is temperature-independent, then  $\gamma_c < 0$  if  $\epsilon > \sqrt{2}$  and capacitance increases at low temperatures at a rate of  $\sim \epsilon \alpha_1$ , (for example, many paraelectrics [22,25]). Ceramics typically have low expansion coefficients ( $\sim 1$  to  $10 \times 10^{-6} \text{ K}^{-1}$ ), while plastics are typically in the range 10 to  $100 \times 10^{-6} \text{ K}^{-1}$ . Total contraction to cryogenic temperatures to 4 K is typically  $< 3\%$  and the last two terms cause a small increase in capacitance on cooling.

However, in many cases  $(\partial \alpha_m / \partial T)_p$  is non-negligible, and this is particularly true of the high-dielectric constant ceramics used in high volumetric efficiency capacitors. Ferroelectric ceramics can have capacitance coefficients of either sign or zero [22]. EIA standards define characteristics and requirements of capacitors, divided up into classes based on stability [26], with Class I having the smallest temperature dependence. Manufacturers meet these criteria by proprietary combinations of a range of ceramics and processes to tune the properties. Class I capacitors are usually based on the paraelectric TiO with admixtures of other materials such as MgNb<sub>2</sub>O<sub>6</sub> and ZnNb<sub>2</sub>O<sub>6</sub> to adjust the temperature characteristics, while Class II components are based on the ferroelectric BaTiO<sub>3</sub> [27]. The diversity of types is required because low temperature coefficient high volumetric efficiency are conflicting requirements in current technology.

Polymer film based capacitors tend to be reasonably stable in temperature but the relative dielectric constant is typically of order 2, making them relatively bulky compared to the ceramics.

Although the contribution to temperature dependence of capacitance due directly to dimensional changes, as discussed above, is relatively straightforward and slowly varying at low temperature, the polarizability is not so well characterized. Experimental data are therefore necessary to ascertain the variation of capacitance down to the expected operating temperatures.

There is a large variety of capacitors available, so the selection tested here is a small subset with some particular requirements. The two types required were a wire-bondable capacitor of about

10–100 pF, and a surface mount capacitor of around 100 nF. The small capacitor should have an area of  $0.35 \times 0.35 \text{ mm}^2$  or less, and a resonant frequency above 10 GHz, while the larger one should operate into the megahertz region and be smaller than about  $3 \times 1.5 \text{ mm}^2$ .

An obvious choice is ceramic capacitors which come in small surface mount sizes and low temperature coefficients. The most stable ones are designated by industrial standards as NP0 or, equivalently, COG [26]. In the 0805 footprint ( $0.2 \times 0.13 \text{ mm}^2$ ) the largest capacitance available is 47 nF. A somewhat worse temperature specification is X7R [26], which may be found in the 0805 form factor with capacitances up to 10  $\mu\text{F}$ . Silicon capacitors are also potentially interesting since silicon has a simple structure that does not change dielectric constant significantly with temperature. Another type of capacitor is based on metalized polymer films. At least one company, Panasonic [28], manufactures SMT capacitors up to 150 nF in a 0805 package (but the data sheets give no information about the specific dielectric material other than ‘plastic’).

Based on the above criteria, a sample of different capacitor types, listed in Table 3, was tested down to 4 K with a Leader LCR-745 LCR meter [29] at 1 kHz excitation frequency. The lead capacitance was negligible for the larger capacitors, but was very significant compared to the smallest capacitances. To determine it as accurately as possible, the total capacitance of the test device plus stray capacitance was measured over the full temperature range. The wiring capacitance was measured separately, and the component capacitance could be ascertained to the larger of about  $\pm 0.2 \text{ pF}$  or  $\pm 1\%$ .

Some of the capacitors were measured at only room temperature, 77 K, and 4.2 K. This was sufficient to characterize the stable types, but the more variable ones were determined over a range of temperatures as the Dewar warmed up. This took several hours, and readings were taken manually at irregular intervals. Since the temperature was constantly changing, there may have been an appreciable discrepancy between the temperature of the sensor and that of the test device. In the context of this work this error is not significant.

Results of the measurements are shown graphically in Fig. 2. Most of the selected components maintained their capacitance quite effectively down to 4 K. The highest capacitance for a 0805 package at cryogenic temperatures is the Panasonic film capacitor. The 150 pF version was not available from stock for these tests, but presumably it would have a capacitance  $> 100 \text{ pF}$  at 4 K. At the low end, the very compact 51 pF capacitor loses almost all its capacity, while the physically larger 47 pF and 15 pF capacitors marginally increase capacitance. In general, it appears that low to moderate dielectric constant materials (6–200) are stable, while high dielectric constant materials (200–14,000) are very susceptible to temperature changes, in agreement with the earlier discussion.

### 3.3. Diodes

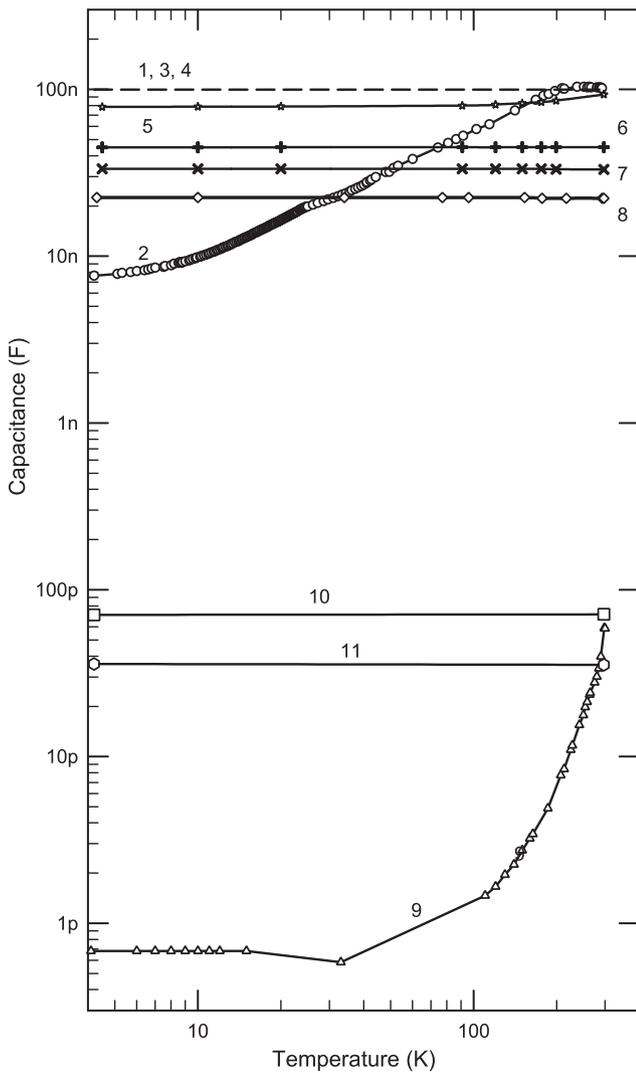
Protection against over-voltages requires a non-linear device such as a semiconductor diode. Diodes typically have a current-voltage characteristic, based on the Shockley theory [35], given by:

$$I = I_s (\exp(e(V - IR)/nKT) - 1), \quad (5)$$

where  $I$  is the current through the diode,  $e$  is the electronic charge,  $V$  is the voltage across the terminals,  $R$  is the diode series resistance,  $k$  is Boltzmann’s constant,  $n$  is an empirical ideality constant, and  $T$  is the junction physical temperature.  $I_s$  is the saturation current, which is also a function of temperature. Diodes are often regarded as having a knee or turn-on voltage that is around 0.3–0.7 V depending on material. However, (5) has no voltage-specific discontinuity, and the effective turn-on voltage depends on the range of currents of interest and the saturation current. The practical

**Table 3**  
Capacitors tested for the bias protection circuit.

No.	Manuf.	P/N	Value	Breakdown voltage (V)	Tol.%	Temp. coeff.	Package	Type
1	TDK [30]	CGJ5L2C0G1H104J	100 nF	>100	±5	C0G, NP0	1206	Ceramic
2	TDK	C1608X7R1C104K	100 nF	>40	±10	XR7	0603	Ceramic
3	IPDiA [31]	935131425610	100 nF	11	±15	<±0.5% –55–150 °C	0603	Silicon
4	IPDiA	935121424610	100 nF	11	±15	<±0.5% –55–150 °C	0402	Silicon
5	Panasonic	ECP-U1C104MA5	100 nF	>16	±20	<±5% –40–80 °C	0805	Film
6	KEMET	C0805C473J3GACTU	47 nF	63	±5	C0G, NP0	0805	Ceramic
7	TDK	C2012C0G1E333J125AA	33 nF	>25	±5	C0G, NP0	0805	Ceramic
8	Murata [32]	GCM21B5C1H223JA16L	22 nF	>50	±5	C0G, NP0	0805	Ceramic
9	Dielectric Labs [33]	D10BV510M5PX	51 pF	>50				
10	Skyworks [34]	SC04701518	47 pF	100	±20	50 ppm/°C	0.71 mm × 0.71 mm	thin film
11	Skyworks	SC01500912	15 pF	100	±20	50 ppm/°C	0.47 mm × 0.47 mm	thin film



**Fig. 2.** Change in capacitance of the capacitors as a function of temperature. Numbers correspond to the indices in Table 2. The recorded temperature may be slightly different from the temperature of the capacitor itself since the temperature was rising continuously, though slowly.

turn-on voltage result from typical bias currents, of order 1 mA, and  $I_s$  is of order 1 pA.

Saturation current magnitude and functional dependence on temperature varies with materials and diode type. For *pn* junctions it is given by [36]:

$$I_s = eAn_i^2 \left( \frac{1}{N_a} \sqrt{\frac{D_n}{\tau_{n0}}} + \frac{1}{N_d} \sqrt{\frac{D_p}{\tau_{p0}}} \right), \quad (6)$$

where  $A$  is the cross-sectional area  $D_{p,n}$  are the diffusion coefficients of holes and electrons, respectively,  $N_{d,a}$  are the donor and acceptor concentrations at the  $n$  and  $p$  sides, respectively, and  $n_i$  is the intrinsic carrier concentration in the semiconductor material.  $\tau_{p,n}$  are the carrier lifetimes of holes and electrons, respectively. Temperature dependence is through  $n_i^2$ , which is proportional to  $\exp(-E_g/2kT)$  for a band gap energy  $E_g$ , and through  $N_{d,a}$ . The latter are fairly constant at higher temperatures, but decrease below  $T = E_a/kT$  where carrier freeze-out starts to occur. The excitation energy,  $E_a$ , depends on the semiconductor and dopants. Si has activation energies that are several times those of Ge and GaAs, so reduction in conduction occurs at higher temperatures, typically  $\sim 120$  K, compared to  $< 20$  K.  $D_{p,n}$  and  $\tau_{p,n}$  also contribute to some extent to the temperature dependence.

Schottky diodes have a saturation current [37].

$$I_s = A^* T^2 S \exp(-\phi_B/kT), \quad (7)$$

where  $A^*$  is the modified Richardson constant,  $S$  is the metal–semiconductor contact area and  $\phi_B$  is the barrier height. The barrier height can decrease by a factor  $> 5$  down to cryogenic temperatures, accompanied by an increase in the ideality factor,  $n$ , by a factor of  $\sim 3$  [38].

Meyaard et al. [39] have studied the temperature dependence of the forward voltage of GaInN LEDs down to 80 K, based on the work of Xi and Schubert [40]. They found that at low temperatures the voltage sensitivity to temperature was much higher than at room temperature ( $-8$  mV  $K^{-1}$  vs  $-1.7$  mV  $K^{-1}$ ) as tunneling became more significant relative to the thermionic emission mechanism of Eq. (5).

In addition to the basic device physics above, other factors that influence thermal effects are the temperature dependence of the series resistance, and the thermal time constants of the diode and packaging. Series resistance can increase drastically at low temperatures, both from the semiconductor conductance and the Ohmic contact [39,41], so low room-temperature resistance devices should be preferred.

Zener diodes will not be considered here. The minimum commercial voltage is 1.8 V. At this voltage, the Zener effect predominates and has a negative temperature coefficient.

From the huge range of potential devices, we selected a few to test based on the manufacturers' data sheets. Criteria that were considered included forward resistance and forward voltage. Silicon *pn* junctions were avoided but Schottky diodes considered. Materials with low carrier freeze-out, such as GaAs were preferred. The results included a number of LEDs and GaAs diodes, as well as

some silicon diodes specifically designed for rectification or circuit protection.

Measurements were made at room temperature (297 K), at 77 K in LN, and at 4.2 K in a closed-cycle refrigerator. A Keithley 2401 Source-Measurement Unit [42] was used to trace the dc IV curves which were then corrected for the measured lead resistances.

### 3.3.1. LEDs

LEDs tested are listed in Table 4. Although obsolete, the Siemens RL55 diode was included since it has been used in a large number of cryogenic amplifiers in the past. The remaining diodes were selected based on their room temperature dc characteristics.

Plots of the device IVCs are divided into visible and infrared groups shown in Figs. 3 and 4, respectively. The most promising for cryogenic operation seems to be the now-obsolete RL55. All of the others exhibit significant increases in their turn-on voltage, and several have voltages that increase by a factor of a few, especially at ~4 K. The back bending of the curves is due to self-heating. This was particularly evident when the devices were immersed in LN since there was an associated rapid boil-off of the nitrogen with the insulating Leidenfrost effect causing the elevation of temperature. This effect will cause an underestimate in the actual diode voltage for pulses that are shorter than the thermal time constant of the diode. No tests were made on this aspect of the characteristics. Incidentally, there was no perceptible change in the color of the LEDs, but the brightness was significantly higher at 77 K, presumably because of a combination of increased efficiency and higher voltage for the same current.

Of the infrared diodes, the SIR19-21C/TR8 is potentially useful if the required clamping voltage is ~2 V.

### 3.3.2. Other diodes

Included in this section are devices specifically designed for ESD (electrostatic discharge) protection, Schottky rectifiers, and as GaAs signal diodes. Many of the component data sheets do not specify the semiconductor material, but we presume that those are all silicon-based devices. Although it was expected that silicon devices might not work well at cryogenic temperatures because of carrier freeze-out, several devices were included in the list of devices tested as they are the most readily available and least expensive (see Table 5).

Unipolar diode results are shown in Fig. 5. All of these had significant forward-conduction even at 4 K, so carrier freeze-out does not seem to be important, presumably because the carriers are produced by impact ionization rather than thermal excitation. Some diodes exhibited the back bending effect, again probably attributable to self-heating. The lowest forward turn-on voltage is associated with the DFLS130L-7 Schottky diode. This has a large current-handling capability even at room temperature. It is likely

from the construction with wide pads that it has low series inductance that will allow fast transients to be clipped by the diode. The relatively large capacitance (~50 to 100 pF) is also helpful in bypassing fast spikes.

A second group of diodes has conduction in both directions (reverse-breakdown diodes, or anti-parallel pairs), and these are represented in Fig. 6. The anti-parallel GaAs diode pair, MA4E1318, has a low conduction voltage that is temperature independent, and these could be very useful where size is important enough to warrant the higher cost and more complex bonding to the circuit.

Two devices that are interesting for forward overvoltage protection are the VESD01-02V-G-08 transient-voltage suppression (TVS) diode, and the SP1001-02JTG TVS diode array. Although the curves for the latter are more suited to our application, the packaging is not as convenient. It comprises several diodes that are connected in such a way that only one can be used. The larger size of the package is also a barrier to its use. The reverse conduction of the VESD01 is at too high a voltage for our specifications, so another device has to be used in parallel for reverse-voltage protection.

### 3.4. Fuses

Fuses are potentially useful for protection against sustained over-current. A surface mount fuse with a rating of 50 mA (AVX [53] F0402G0R05FNTR) was tested at room temperature and 4.2 K. Characteristics are shown in Fig. 7 for several samples and different rates of change of current. Although the temperature affects the burn-out current, the rate of change of current seems a more significant determinant. These fuses could be useful in situations where the non-linearity and time dependence are not a problem, but they are too slow for most protection requirements.

### 3.5. Connectors

For connectors, the primary qualification is the ability to withstand thermal cycling. We wanted a connector with at least ten pins that could be surface mounted on a PCB. It had to be small to fit in the form factor of the block, be polarized to avoid insertion in the wrong polarity, and have a positive locking mechanism. The two that were eventually selected as candidates were a 15-pin Nano-D connector from Cristek [54], and a 10-pin rectangular ST connector from Hirose [55]. The Cristek board connector (SRN1-15S-TP-T) is a single-row right-angle stainless steel shell part, while the mating connector (CMN1-15P-JPT001) also has a metal shell, as well as 0–80 UNF capture screws, and pigtailed to attach cryogenic wires. The Hirose board connector (ST60-10P) has a thermoplastic, glass-reinforced shell, with a metal shield. Its mating connector (shielded ST40X-10S-CV(80); unshielded ST40-10S-CV(80)) also has a glass-reinforced thermoplastic shell. A nice feature is the

**Table 4**  
LEDs selected for cryogenic testing.

No.	Manuf.	P/N	Description	Material	Package
1	Siemens [43]	RL55	Red	GaAs	Radial
2	ROHM [44]	SML-P11VTT86	High brightness red	AlGaInP on GaAs	0402
3	ROHM	SML-P12VTT86	High brightness red	AlGaInP on GaAs	0402
4	Vishay	VLMG1500-GS08	Ultrabright yellow-green	AllnGaP	0402
5	Vishay	VLMO1500-GS08	Ultrabright soft orange	AllnGaP	0402
6	Vishay	VLMS1500-GS08	Ultrabright super-red	AllnGaP	0402
7	Kingbright [45]	APT1608F3C	IR	GaAs	1.6 × 0.8 mm <sup>2</sup>
8	Lite-On [46]	HSDL-4420#011	IR	AlGaAs	2 × 2 mm <sup>2</sup>
9	Everlight [47]	IR19-315C/TR8	IR	AlGaAs	1.7 × 0.8 mm <sup>2</sup>
10	Fairchild [48]	QEB363ZR	IR	GaAs	T-3/4
11	OSRAM [49]	SHF 5050-Z	IR	?	1.7 × 0.8 mm <sup>2</sup>
12	Everlight	SIR19-21C/TR8	IR	GaAlAs	1.6 × 0.8 mm <sup>2</sup>
13	Vishay	VSMS3700-GS08	IR	GaAs	PLCC-2

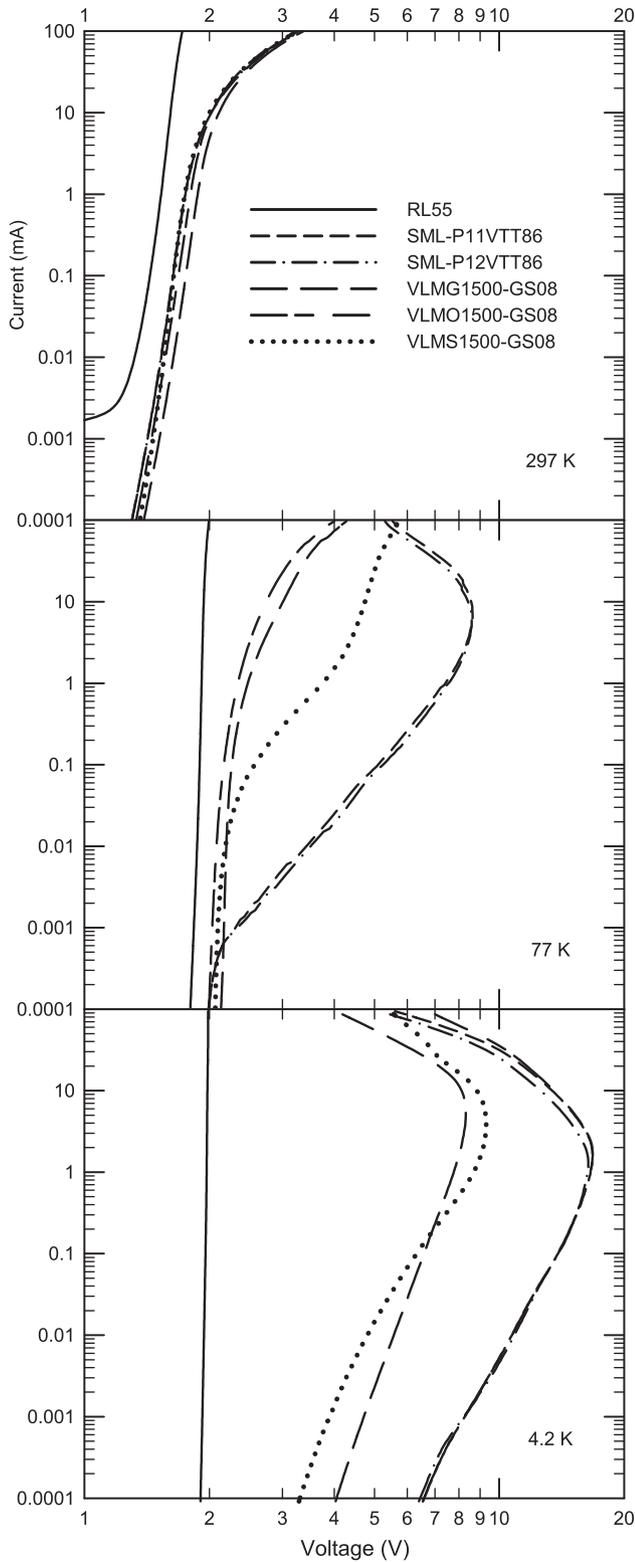


Fig. 3. IV-curves for visible light LEDs.

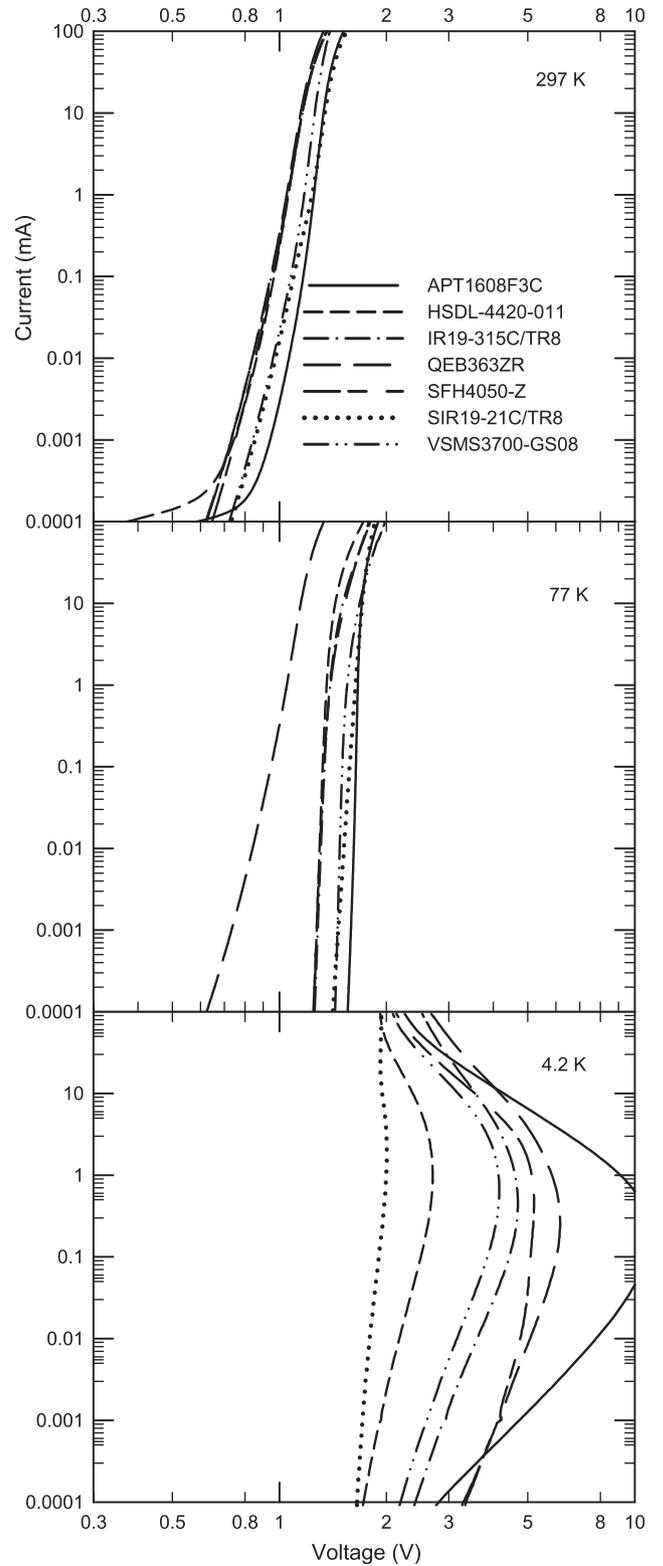


Fig. 4. IV-curves for infrared LEDs.

locking mechanism with a release button on either side that can be easily disconnected.

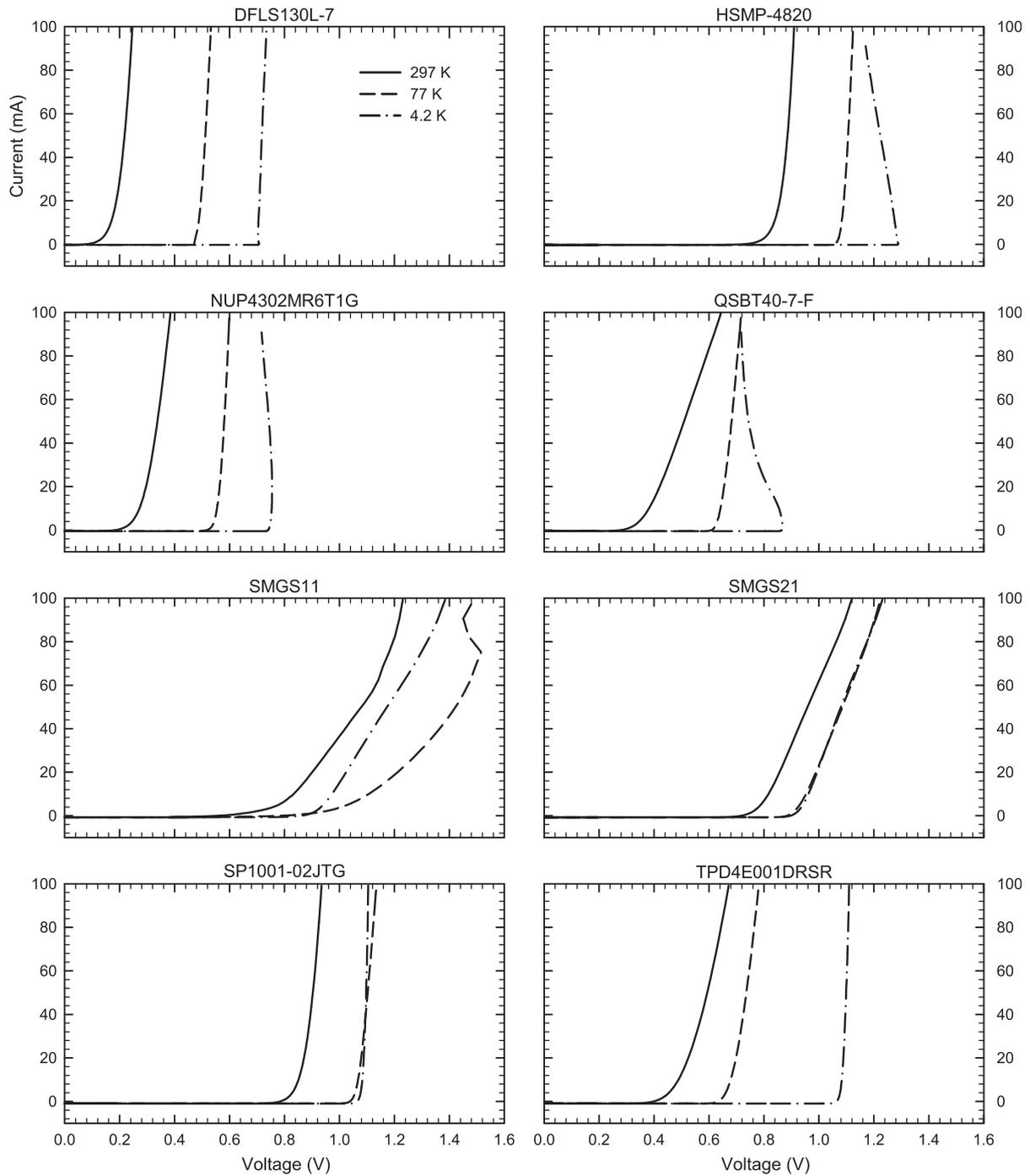
Both types of connector are specified for the military temperature range ( $-55\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ ). Since we had concerns about the durability of the Hirose plastic shell during thermal cycling, we subjected it to >50 thermal cycles by immersing it in LN. The ‘soak’ time in the LN varied from a few seconds to a couple of days.

Warming-up was done in air with no special precautions to avoid water condensing or freezing on the connector. During this time, the contact resistance was monitored and not found to vary. The value was always dominated by the lead resistance to the digital multimeter ( $\sim 0.2\ \Omega$ ).

The Nano-D connector is smaller than the Hirose connector, but the latter is significantly lower in cost and is easier to handle.

**Table 5**  
Non-LED diodes that were tested cryogenically.

No.	Manufacturer	P/N	Description	Material	Package
1	Diodes, Inc. [50]	DFLS130L-7	1A Schottky rectifier	Si (?)	PowerDI®123
5	Diodes, Inc.	QSBT40-7-F	Schottky diode	Si (?)	SOT-363
6	Aeroflex [51]	SMGS11	Schottky diode	GaAs	DFN 0503
7	Aeroflex	SMGS11	Schottky antiparallel	GaAs	DFN 0503
8	Littelfuse [52]	SP1001-02JTG	TVS diode array	Si (?)	SOT-323-3
9	Vishay	VESD01-02V-G-08	TVS diode 1V 63W	Si (?)	SOD-523



**Fig. 5.** IV-curves for unipolar diodes. The negative part of the curves are not shown since they all had insignificant leakage currents, especially at cryogenic temperatures.

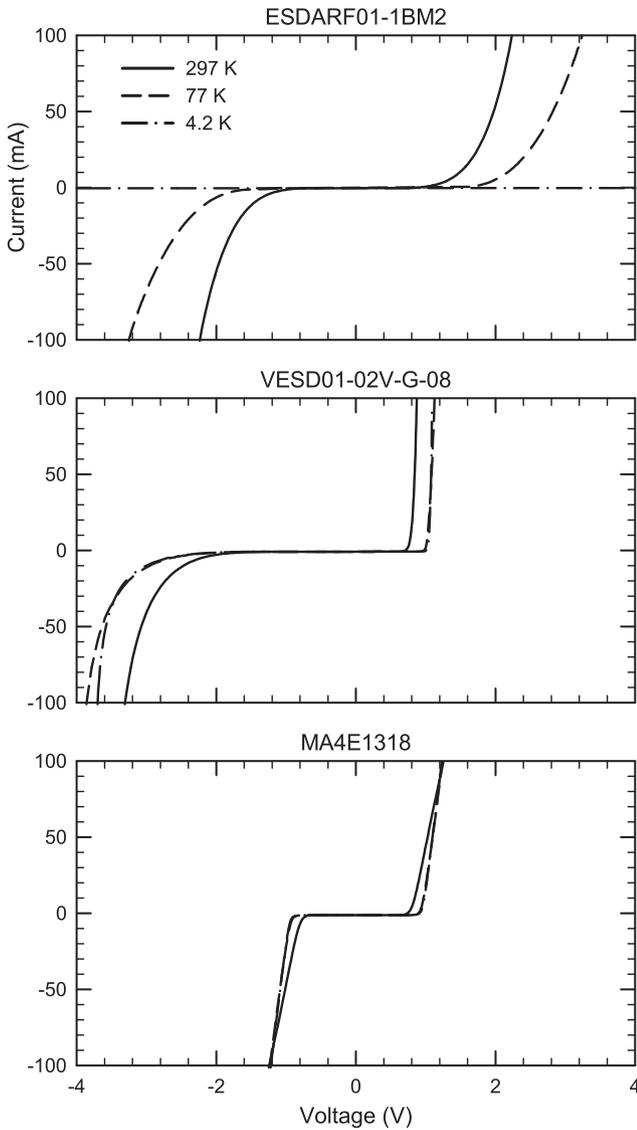


Fig. 6. IV-curves for bipolar diodes, as described in the text.

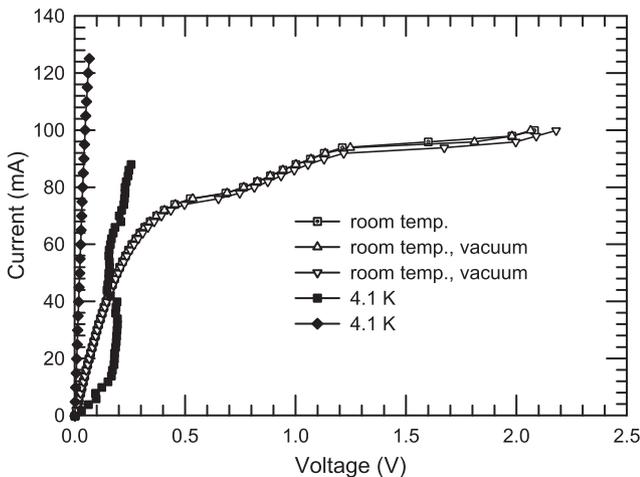


Fig. 7. Current–voltage curves for samples of an AVX F0402G0R05FNTR 50 mA fuse. The curves also depend on the rate of current change in the fuse, and the two curves for 4.1 K correspond to  $2.8 \text{ mA s}^{-1}$  (irregular curve) and  $1.4 \text{ mA s}^{-1}$  (steep curve).

3.6. General comments

The number of devices of each type tested was small so no particular conclusions can be made about reliability. None of them failed due to thermal cycling, and our general experience with small electronic components is that failures are rare, and when they do occur it is often due to stresses applied by connections that can be made more compliant to avoid the problem.

Again, because of the limited number of samples, we cannot comment on the variability of cryogenic performance. There is no assurance that uniformity at room temperature translates to uniformity at low temperatures.

4. Bias protection circuit

Our application for these components is for protection of millimeterwave MMIC amplifiers. These are InP devices with gate lengths of 35 nm operating at drain biases around one volt and gate biases of  $\pm 0.4 \text{ V}$ . Fig. 8 shows the circuit that was adopted based on the preceding component testing. A ratio of ten voltage divider is used in the gate circuit to attenuate external noise and interference. Negligible gate current in normal operation means that the division ratio is set only by the resistors. Gate protection diodes are inserted in the divider network such that their cryogenic turn-on voltage is scaled to a suitable value at the gate. Addition of the 100 nF capacitor provides additional attenuation at frequencies above the cut-off frequency,

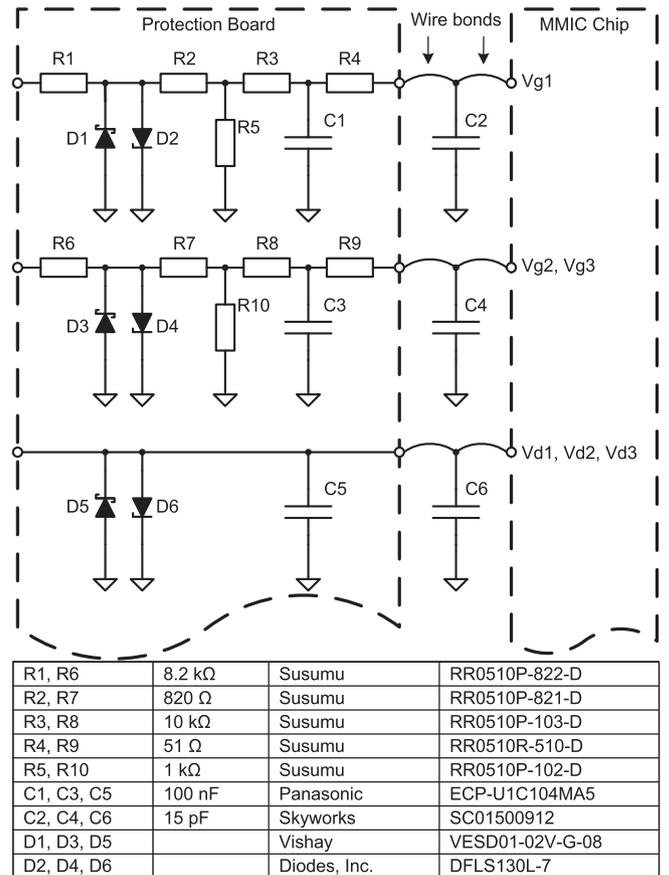


Fig. 8. Protection circuit for one MMIC amplifier chip. The chips that this is designed for has three transistors. All the drains are connected together on chip, and the first transistor has its own gate control, while the other two are connected in parallel. Three such circuits are incorporated on each protection board, one for each of the MMICs in the block.

$$f_c = 1/2\pi R_{\text{eff}} C1. \quad (8)$$

$$R_{\text{eff}} = R3 + R5 - \frac{R5^2}{R1+R2+R5}.$$

The effective attenuation is  $\sim 20$  dB up to about  $f_c = 146$  Hz, after which it increases by 6 dB per octave. The chip decoupling capacitor, C2, ensures a low impedance  $\leq 10 \Omega$  above about 1 GHz.

The drain circuit resistance has to be small to avoid excess heat dissipation so the decoupling capacitor C5 is less effective than in the gate circuit. However, the drain resistance is of order  $40 \Omega$  so the 100 nF capacitor presents a lower impedance at frequencies  $\geq 40$  kHz. This helps in reducing interference from such sources as the dc-dc converters at  $\sim 300$  kHz that are widely used in CARMA.

For the CARMA receivers we will use three chips, each with three HEMT stages, in cascade in a single package. Each MMIC chip requires a single drain supply for the three HEMTs, one bias line for the first transistor gate, and one for the second and third transistor gates which are tied together on the chip. The block that the MMICs are mounted in, along with the input and output waveguide probe transitions and gain slope equalizers, is 25 mm from input to output, so the bias circuit should be narrower than this.

The circuit is laid out on 0.5 mm thick FR4 circuit board. A Hirose ST60-10P connector is used for the bias cable. 0.15 mm wide traces were used for all connections. The traces run into the pads on the diodes and capacitors and out the other side to avoid any inductive stub that would isolate them from very fast spikes that

could then damage the MMIC. Since the connections to the 15 pF capacitor are wire bonds, the conductors were gold plated. The RoHS-compliant solder that is used to mount the components does not result in significant gold leaching and embrittlement.

The envelope of the board is 24 mm by 23 mm, with four holes to mount it to the amplifier block with 0–80 UNF screws. The bottom plane and the top plane between traces are flooded with copper to ensure a good, low-inductance ground plane, and vias are used to stitch the top and bottom together, with at least one via close to each component ground pad.

To verify the circuit, fast voltage steps were applied to the connector and the response at the wire bond pad measured with an oscilloscope. An Agilent 33220A pulse generator [56] was used to generate steps with 5 ns rise times. Since the generator is effectively a  $\pm 10$  V source in series with a  $50 \Omega$  source resistance, a wideband amplifier was used to raise the applied voltage and current. Using a Texas Instruments THS3095 210-MHz bandwidth current feedback amplifier we were able to generate steps from zero to either +25 V or  $-25$  V, and currents up to  $\pm 300$  mA, depending on the load impedance.

Results of these measurements, shown in Fig. 9 for room temperature operation, and Fig. 10 for operation at 77 K in LN, demonstrate that the circuits effectively snub the voltages that would be applied to the MMIC, as required. Because of the extra complication in having long inductive leads going into a closed-cycle dewar

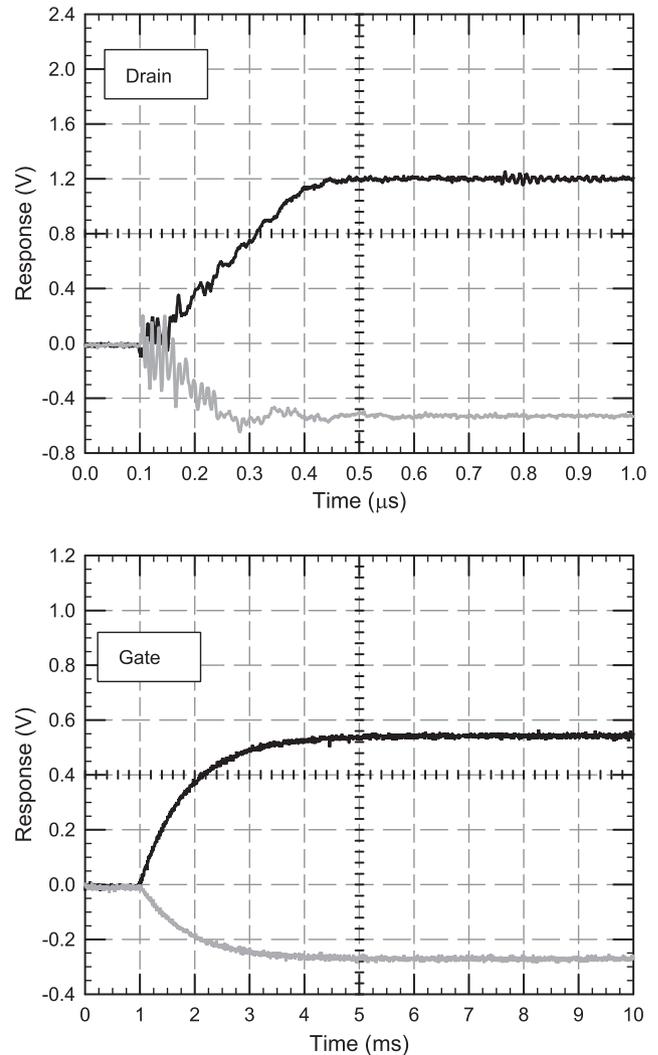
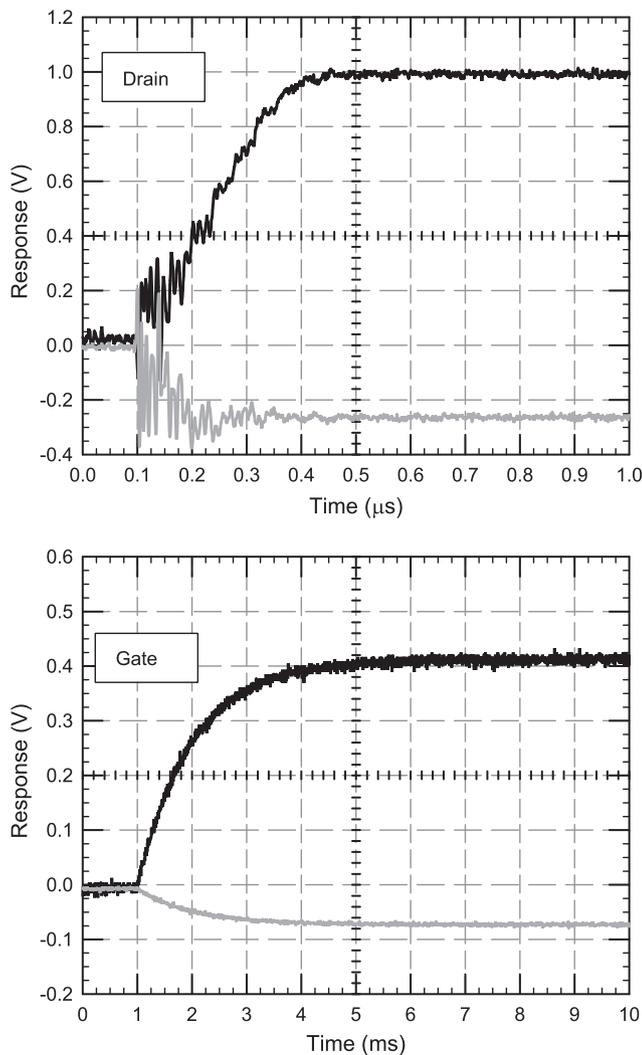


Fig. 9. Response at room temperature of the drain and gate bias protection circuits to  $\pm 30$  V step with a 5 ns rise/fall time.

Fig. 10. Response at 77 K of the drain and gate bias protection circuits to  $\pm 30$  V step with a 5 ns rise/fall time.

we did not do the verification at 4.2 K; all the components were individually well characterized at that temperature so this test was judged not to be essential.

Some ringing is evident in the very rapid pulse response in the drain protection circuit (due mainly to parasitics in the measurement setup), but the peaks are effectively limited by the diode clamp. The rise times for the drain and gate are commensurate with the cut-off frequencies calculated above, which correspond to time constants of 4  $\mu$ s and 1 ms respectively.

## 5. Discussion and conclusions

Measurements of the salient characteristics of many linear and non-linear components were made at cryogenic temperatures as low as 4 K, adding significantly to the data on components that can be considered for bias protection circuits. The linear components generally have simpler behavior with temperature, and it is relative easy to find devices that are very insensitive to temperatures.

Thin-film resistors are available in a variety of sizes of surface mount components. We evaluated samples from only one manufacturer (selected on the basis of cost and availability), but it is expected that the fabrication methods of other manufacturers are similar enough that almost any of them would perform similarly well. For the most part the changes in resistance were of order a percent, though higher resistances appear to suffer larger fractional changes. Although these variations exceed the device tolerances, they are quite acceptable for most applications. Any requirement for higher tolerance would need careful selection. Voltage dividers could be made quite stable if constructed from a single value of component as the relative changes would cancel out, but large division ratios with a high and a low resistance value would not be guaranteed to be temperature insensitive.

Capacitors with low temperature coefficients at ambient generally seem to maintain their capacity at low temperatures very well. In the ceramic family, all the NPO (COG) components performed well. Other ceramic dielectrics did not fare as well, some having changes by a factor of a few. In general, Class I capacitors with dielectric constants  $\leq 200$  are stable, while higher values are increasingly variable. The Panasonic aluminized polymer capacitors prove to be almost as stable as the NPO ceramics, but are available in larger values for the same footprint (e.g., 150 nF vs 47 nF in a 0402 SMT package).

Several semiconductor devices were tested as potential over-voltage protection elements. LEDs have very sharp turn-on characteristics at room temperature, with voltages that are suitable for protecting MMICs. However, at cryogenic temperatures the effectiveness is greatly reduced, especially within a few degrees of absolute zero. Instead, silicon devices especially designed for ESD protection or power rectification proved to be much less dependent on temperature, and we were able to select some that had characteristics suitable for our application.

The extensive set of measurements made here should provide some guidance for other researchers interested in low-temperature, low-voltage protection. Applications vary from laboratory measurements with cryogenic environments to space applications where radiative cooling may reduce temperatures appreciably below the range specified by device manufacturers.

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